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Speech time expansion and compression

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Thesis Advisor: R. W. Adler

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Gültekin Fişek
Lieutenant (junior grade), Turkish Navy
B.S., Naval Postgraduate School, 1972

Submitted in partial fulfillment of the
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December 1972

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Thesis Advisor

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Chairman, Department of Electrical Engineering

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Academic Dean

ABSTRACT

A new variable analog delay principle is used during playback, of pre-recorded speech, to maintain the original pitch when it is played back at half and at twice original recording speed. Original pitch is maintained in speeded up or slowed down speech by expanding or ccmpressing in time, respectively.

A proposed system is described and typical experimental results are provided to illustrate the system performance.

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ACKNOWLEDGEMENT

The author wishes to express his sincere appreciation to his wife, Beyda, for her faith and encouragement, and Dr. Richard W. Adler for his valuable advice and guidance.

I. INTRODUCTION

A. NEED FOR STUDY

The speech time expansion and compression subject has long been studied by people in the audio field. Present solutions of the problem consist of expensive and complex devices, such as analog-to-digital and digital-to-analog converters or a large number of bandpass filters. Thus, there is a need of a simple and an inexpensive circuit.

Only an analog delay line can meet the performance and cost requirements, but has not been available up to now.

A new variable delay line for analog data processing has been realized in integrated circuit form. Its basis is a chain of storage capacitors and charge transfer circuits, acting as an analog shift register with externally variable shift rate. This configuration is known as a Bucket Brigade circuit because of resemblance to a fire brigade of old.

With the arrival of Bucket Brigade concepts, the techniques developed for digital integrated circuits have become adaptable to analog signals. Indeed, the capacity to handle streams of analog signals is basic to growing charge transport technology, which provides elegant integrated versions of a host of electronic functions: audio and video delay, time error correction, time scale conversion, filtering, and imaging.

1. Bucket-Brigade Electronics

The 'Bucket-Brigade' is an analog shift register which transfers information from stage to stage in response to timing signals [1].

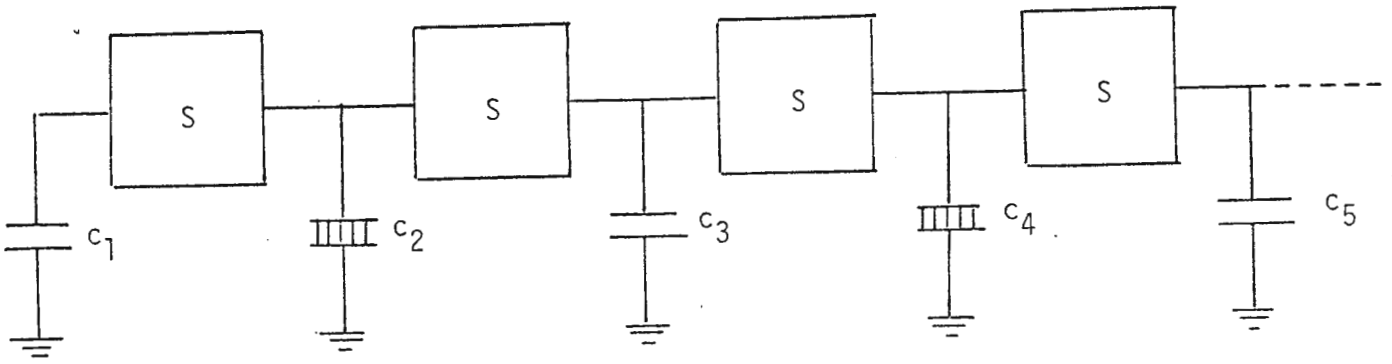
It replaces more expensive and elaborate techniques of creating long audio delays. These include specially designed tape recorders,

with rotating playback heads and digital stystems that convert the analog signal to digital form, delay it in digital shift registers, and convert it back into an analog signal.

The principle of operation of the Bucket Brigade is that the signal to be delayed is sampled and stored in a cascade of capacitors interconnected by switches operated at the same frequency as the signal sample.

As a new signal sample can obviously not be stored in a capacitor before the signal sample present is completely removed, only half the number of capacitors do store information at any moment, the others being empty. This is illustrated in Fig. 1. In Fig. 1.a the even numbered capacitors are assumed to contain signal samples and in Fig. 1.b these signal values are transferred to the odd numbers accompanied by the entry of a signal sample at the input and the delivery of a signal at the output. Odd and even numbered switches are driven with a sampling period phase difference.

This type of delay line never came into general use nor did the design become standardized, because the switches S were far more complicated and bulky than the inductances they were to replace. It should be noted that the function of S is much more sophisticated than that of a normal switch. It must be guarantee a correct and complete transfer of signal sample, preferable unaffected by nonuniformity of the storage elements and free from losses, nonlinearity, and residual storage effects. In the past only rather complicated circuitry has been proposed for this function, so that even in integrated compact form there was no change in the expense of the design.



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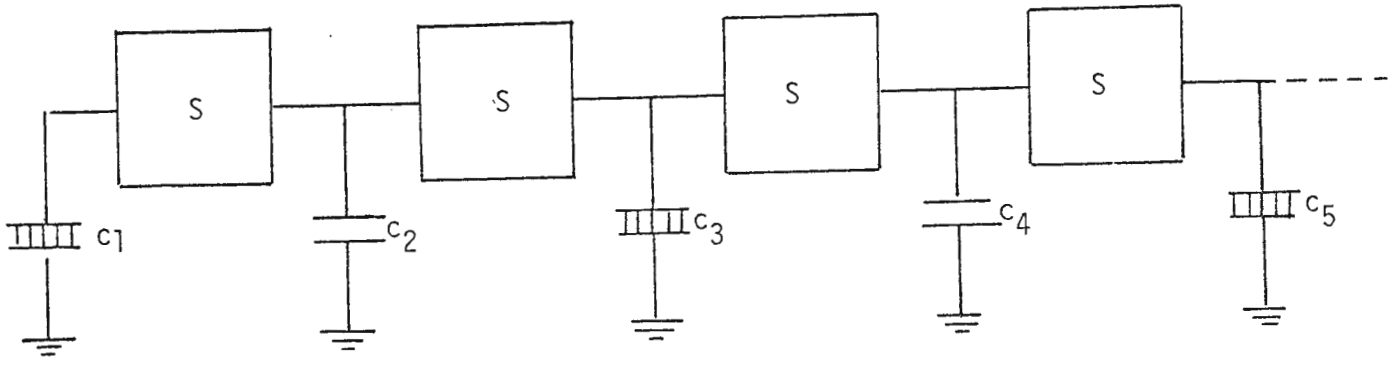


(b)

Figure 1. Principle Configuration for an Analog Shift Register.

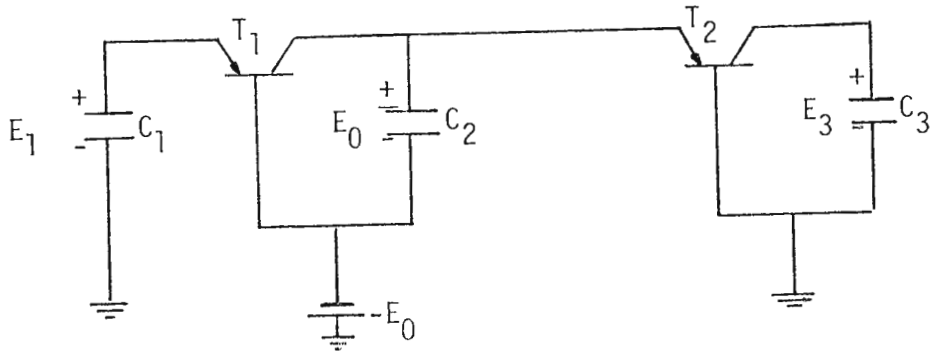
A much simpler solution occurs when signal sample transfer is not established by a charge transfer in the direction of signal travel but in the opposite direction, by what is essentially a charge deficit transfer. This principle leads to a much simpler resistorless circuit suitable for realization in integrated circuit form.

The basic circuit and its functions are illustrated in Fig. 2. In Fig. 2.a, capacitor C_1 is assumed to have a voltage E_1 representing a signal sample. The base of transistor T_1 is at a potential $-E_o$, the capacitor C_2 has a voltage E_o, so that the collector of T_1 is at zero potential and T_1 is in a nonconductive state. Capacitor C_3 stores a preceeding signal sample represented by a voltage E_3. All signal samples are assumed to be smaller than E_o.

Now the base of T_1 is switched to a potential $+E_o$ (like all other odd transistors in the array). The base-emitter junction is conducting and current will flow to C_1 until its potential reaches $+E_o$ (junction bias voltage is neglected). The collector-base junction remains reverse biased so that T_1 acts as a linear common-base amplifier.

The charge $\Delta q=C_1(E_o-E_1)$ fed back to C_1 is almost wholly delivered by the T_1 collector current. The result is that C_2 is discharged to a voltage $E_o-\Delta q/C_2$, which is E_1 for $C_1=C_2$.

Capacitor C_3, in the same situation as C_1, is also charged to E_o (Fig. 2.b). In the next half of the sample interval the base of T_1 is switched to $-E_o$ and a similar charge transfer takes place from C_3 to C_2; the forward biased transistor T_2 brings the collector of T_1 to zero potential. Thus C_2 is recharged to the voltage E_o and during this time Δq is withdrawn from C_3 (Fig. 2.c).



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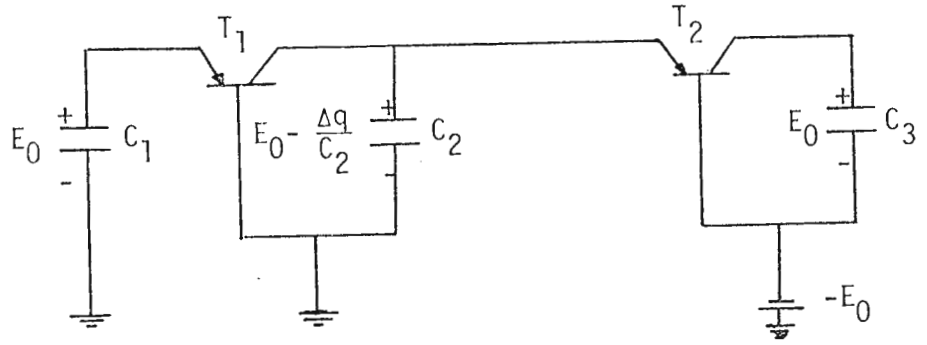

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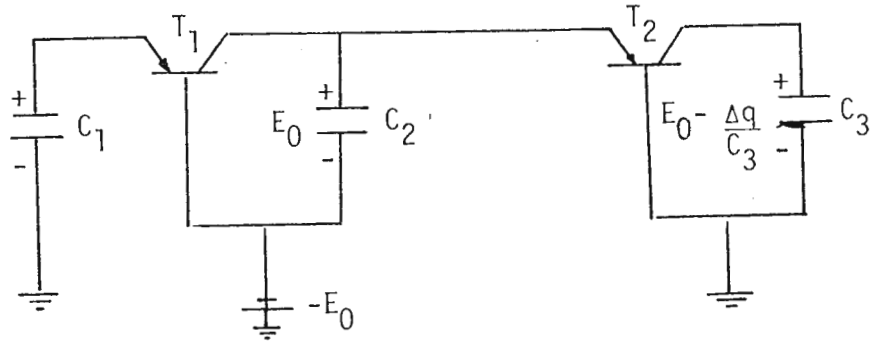


(c)

Figure 2. Principal Operation of the Bucket Brigade Line with Charge Deficit Transfer.

The sampling interval is now complete and we see that the information is transferred from one odd capacitor to the next odd one by the charge deficit replenishment.

In MOS technology, the Bucket Brigade concept leads to an even simpler configuration than is possible in bipolar technology [2]. Input and output circuits with fewer components are possible. Due to the absence of gate currents, attenuation is negligible even after hundreds of stages, and no amplifiers are necessary. Fig. 3 represents a complete MOS delay line. Here, the delay line uses two complementary clock signals with a frequency equal to the sampling frequency applied to the input signal. Functionally, the device provides a delay line in which bandwidth and delay can be interchanged between limits. Signal delay can be accurately controlled or if needed, can be changed electronically. Since the clock frequency is equal to the smpling frequency, according to Nyquist Sampling Theorem, these clock signals are limited by the input signal bandwidth. The minimum sampling frequency for adequate representation of a signal of bandwidth B is 2B. Then the minimum number of memory cells required for a delay T is basically,

$$n=2f_cT \quad \text{or} \quad n=4BT,$$

where n=Number of bits in the Bucket Brigades

f_o=Clock frequency

T=Delay time

B=Bandwidth

Since only half the number of capacitors actually do store information at any moment the constant 2 appears at the above formula.

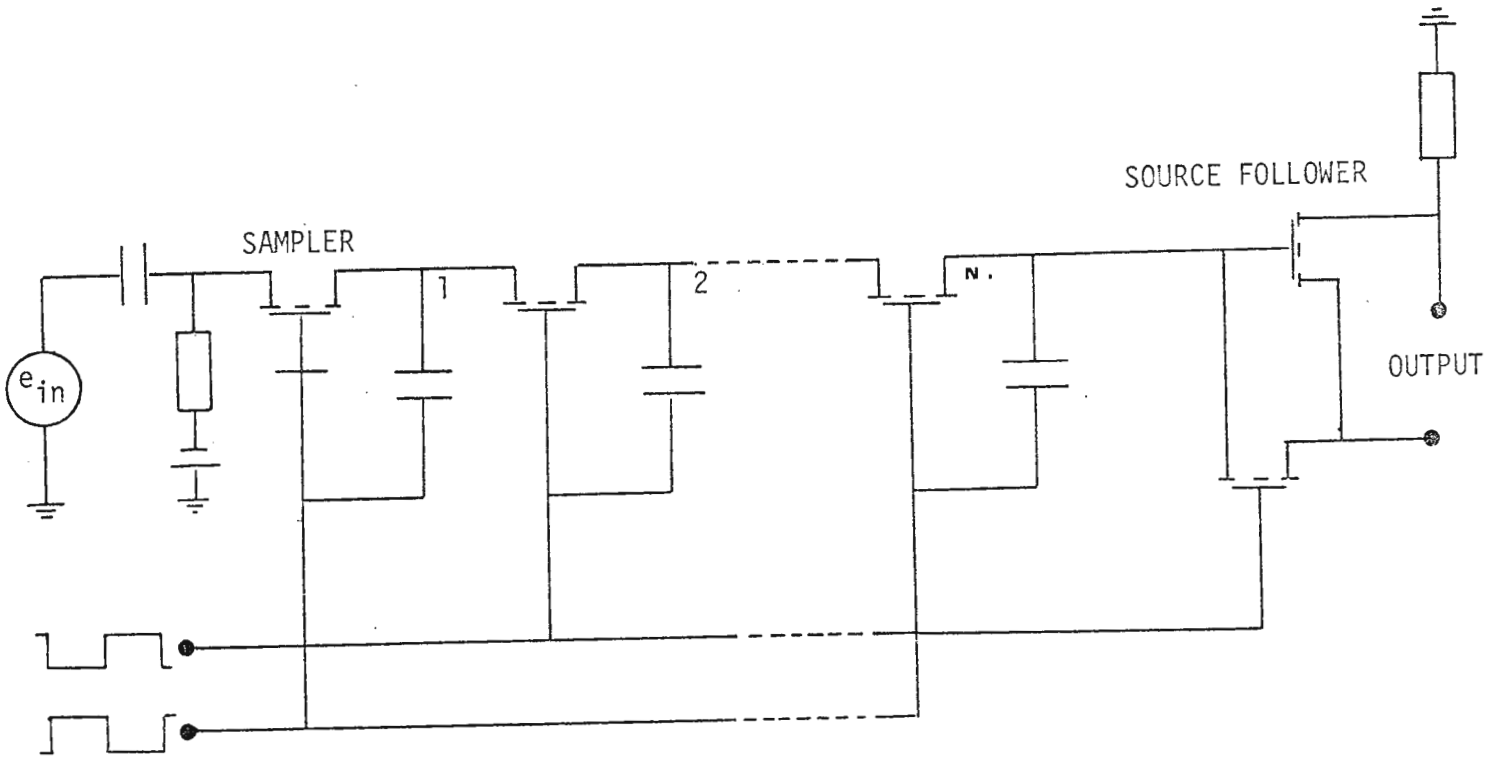


Figure 3. Circuit Configuration of a MOS Delay Line.

B. STATEMENT OF THE PROBLEM

When a tape recorder is played back at speeds greater than its recording speed it produces high-pitched distortion. That is if the tape is played with the speed greater than the original recording speed by a factor of two, the fundamental frequency of the original signal is doubled (Fig. 4). Conversely for a tape played at a half speed, the fundamental frequency of the original recording is expanded by a factor of two. The decision rule is that the change in fundamental frequency of the originally recorded signal is directly proportional to the change in the playback speeds.

The purpose of this study is to establish the feasibility of a low cost circuit for the expansion and compression of pre-recorded speech to its original fundamental frequency when it is played back at faster and slower speeds.

C. PROPOSED APPROACH

In the solution of the problem Bucket Brigades are used as storage devices. Two of them are time division multiplexed. The output of the tape recorder is sampled and these samples are stored in one of the Bucket Brigades with an appropriate clock frequency while the contents of the other one are read out with a clock frequency depending upon playback speed. Of course read and store time can be adjusted and changed electronically by controlling the clock frequency of each Bucket Brigade. Due to the time division multiplexing process, each Bucket Brigade is switched in two different modes of operation.

1. Store Mode

In this mode of operation, sampling and clock frequencies are made equal. The output of the tape recorder is sampled at the front

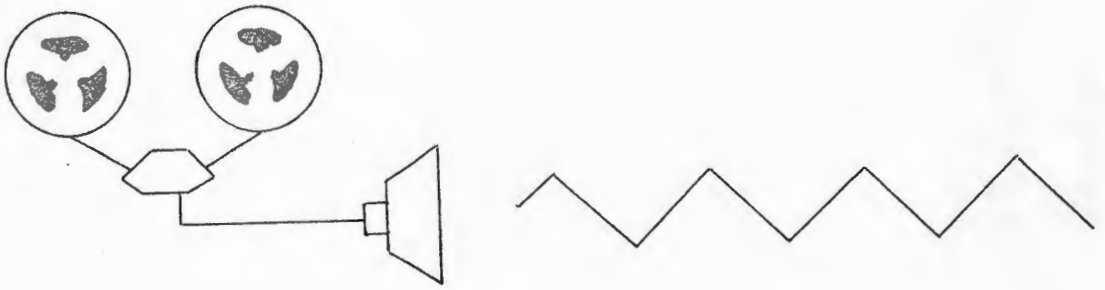


Figure 4.a. Normal Signal Transmission.

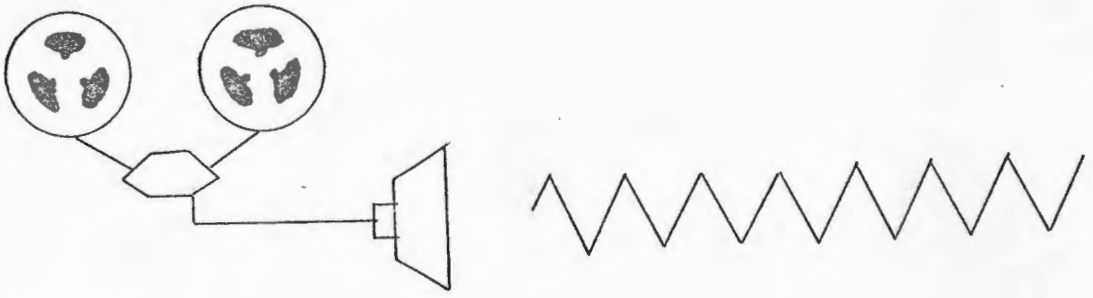


Figure 4.b. Accelerated Signal Reception.

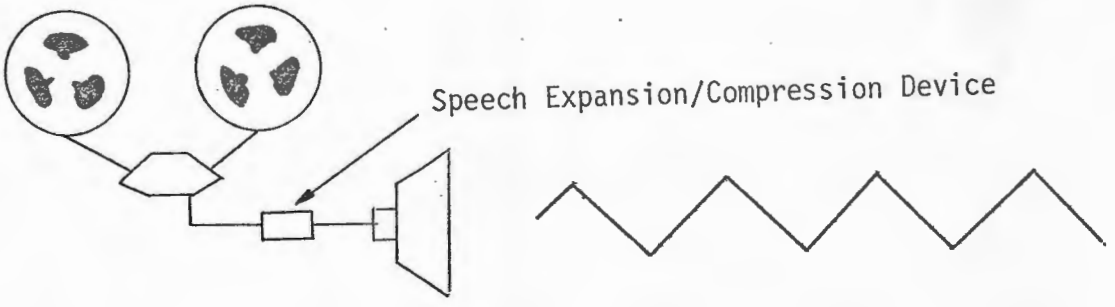


Figure 4.c. Accelerated or Decelerated Signal Reception with Normal Pitch.

end of the Bucket Brigade, and first sample is stored in the cell by the first clock pulse. When the second clock pulse is applied, a second sample is stored in the second cell, and the contents of the first cell are transferred to the third one by charge deficit transfers. Then by each clock pulse, the samples are transferred to successive cells. The time required to store the samples in the cells of the Bucket Brigade is:

$$T=n/2f_c$$

2. Read Mode

After the samples are stored in the Bucket Brigade it is switched to the read mode of operation. (The output of the tape recorder is then switched to the other Bucket Brigade which is in the store mode.) In the read mode of operation, the clock frequency is adjusted according to the playback speed of the tape recorder. (When the tape is played back at twice the recording speed, signal time compression results, that is, the fundamental frequencies are doubled.) This compressed signal was sampled and stored in the first Bucket Brigade at a clock frequency f_c. In the read mode the clock frequency is switched to $f_c/2$, which is equal to half of the store clock frequency. The contents of the cells are then transferred toward the output at a slower rate. This results in signal time expansion. Thus, in the read mode, pre-compressed signals are expanded in time to form the originally recorded signal.

Fig. 5 represents the form of signal at the input and output of the Bucket Brigade. In Fig. 5.a, the signal output of the tape recorder is divided into time frames. Each time frame is equal to the storage time. Since the store and the read time are not equal, the

even numbered signal frames are deleted during the multiplexing process. Fig. 5.b shows the remaining signal wave at the output of the Bucket Brigade, which is reshaped to normal pitch.

In reverse, when tape recorder is played at half speed, then the read clock frequency is increased to $2f_c$. So, pre-expanded signal samples are compressed in the read mode of operation by the high-rate clock pulses.

Figure 5.c shows the output of the Bucket Brigades, when the tape is played by a half speed. Since the store time is greater than the read time, there exists an empty signal time frame.

D. REVIEW OF RELATED WORK

In the past an electronic device to allow "speed hearing" of recorded speech at word rates comparable to speed reading was developed by Bell Telephone Laboratories [3]. Designs for the device, called the Harmonic Compressor, have been given to the American Foundation for the Blind for possible use in making recordings for the blind.

The harmonic compressor permits making recordings of human voice which can be played at twice their normal speed while retaining normal voice pitch. The device eliminates the high-pitched babble that results when an ordinary record is speeded up.

The harmonic compressor works in this manner: Speech is fed to a bank of 36 bandpass filters which separates the speech into its frequency components. The output of the bank of filters is sent, in turn, to 36 frequency dividers which halve the frequencies of the narrow-band signals from the filters.

From the dividers, the halved frequency singals go to networks which remove distortion and combine the 36 halved signals into one

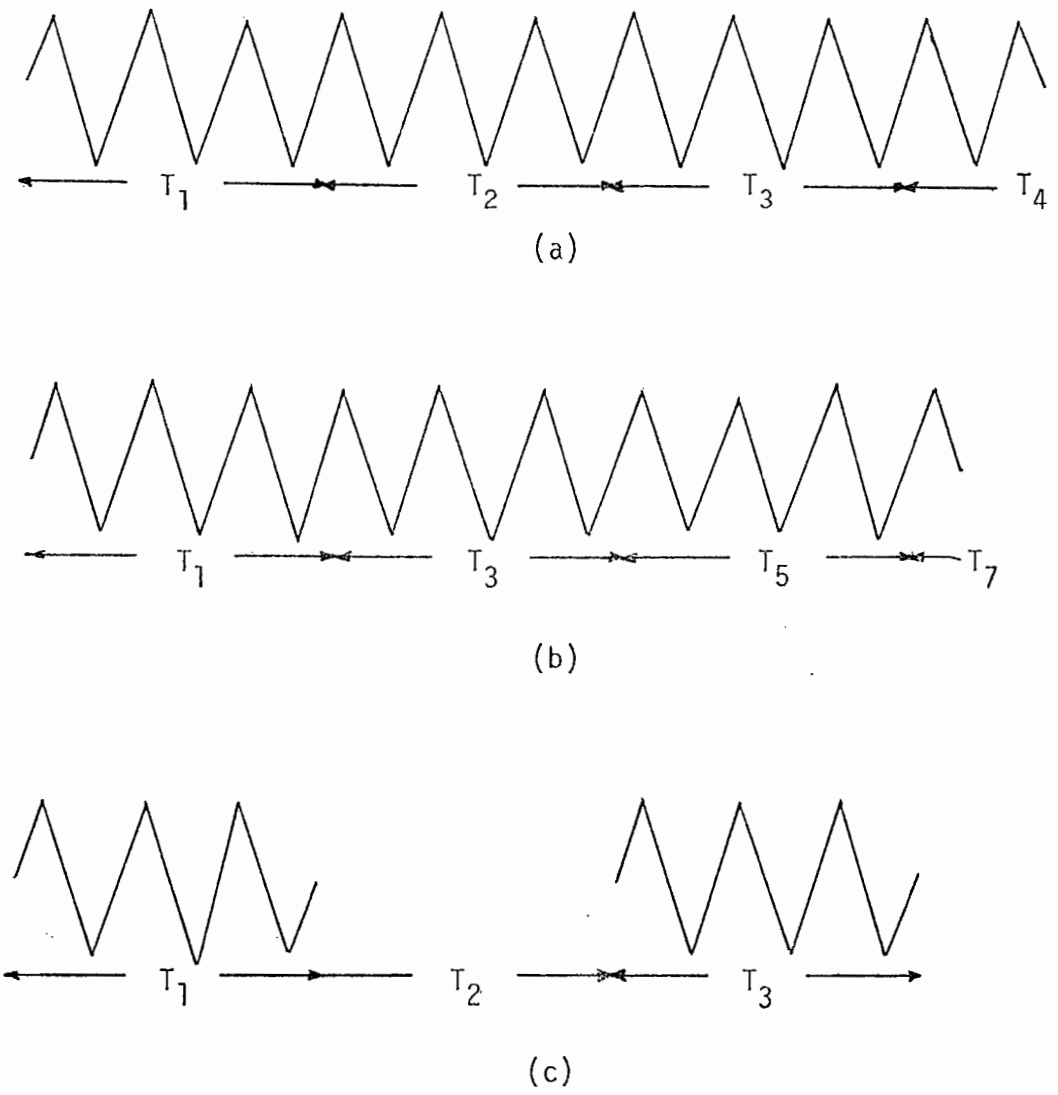


Figure 5. Signal Wave Forms at the Input and Output of the Bucket Brigades.

signal. The frequency components of this signal are then half of the original input values. This "harmonically compressed" signal is recorded on magnetic tape.

The halved frequencies are restored to their original values by doubling the playback speed. Syllabic rate is then doubled without doubling the speech.

Figure 6 represents the complete block diagram of the Harmonic Compressor.

The system described above has many disadvantages. Due to the large number of components, such as band pass filters, modulators, and dividers, the cost is very high. Also, this system is incapable of expansion of the speech in time.

The other system which has been used to compress and to expand the pre-recorded speech uses a magnetic tape recorder which has rotating heads. The rotation speeds of these heads can be adjusted externally. Thus, to compress the analog signal, the tape was played back at twice speed, and the rotation speeds of the heads were adjusted to the recording speed. Due to the slower rate of reading, the signal samples form the original analog signal. (Again, the deleted time frames occur during compression.)

Conversely, to expand the given analog signal, the tape was played back at half speed, and the rotation of the heads were kept in their original speed.

In this method, the need of the rotating heads increases the cost very much.

In addition to the Harmonic Compressor and the Tape Transport approach for speech time compression and expansion, a Buffer shift

register with feedback control has been used to obtain a variable time delay in tape recordings not for speech time compression or expansion but, to compensate playback time base error (TBE) [4]. The primary source of the base error is the instantaneous velocity variation in the magnetic tape. To compensate the TBE of a recorded signal, the data signal and a constant frequency pilot signal are recorded on separate channels of the recorder. If the tape skew effects are negligible, both signals have the same time base perturbation on playback. Sampling the playback signal at times corresponding to the leading edges of the perturbed pilot signal is equivalent to uniform sampling of the original data signal in the absence of TBE. Consequently, the original data signal can be recovered by sending the sample values at a uniform rate to the appropriate reconstruction circuit. Since the sampling rate must be several times the nominal bandwidth of the data, the recorder must have sufficient bandwidth to accommodate the pilot signal. Alternatively, a low frequency pilot signal can be recorded, and then multiple of this signal is used during playback to control sampling.

The system is implemented as illustrated in Fig. 7, by converting the sample values to digital form using an analog-to-digital converter, and storing them in a shift register. The samples are then clocked out of the register at the normal sampling frequency and converted back to analog form by a digital-to-analog converter. The original signal is reconstructed by smoothing the output with a low-pass filter.

The main purpose of the buffer control loop in Fig. 7 is to sense the tendency of the buffer to overflow or underflow and to increase or decrease, respectively, the voltage controlled-oscillator (VCO) frequency which controls the buffer output rate. In addition, the loop

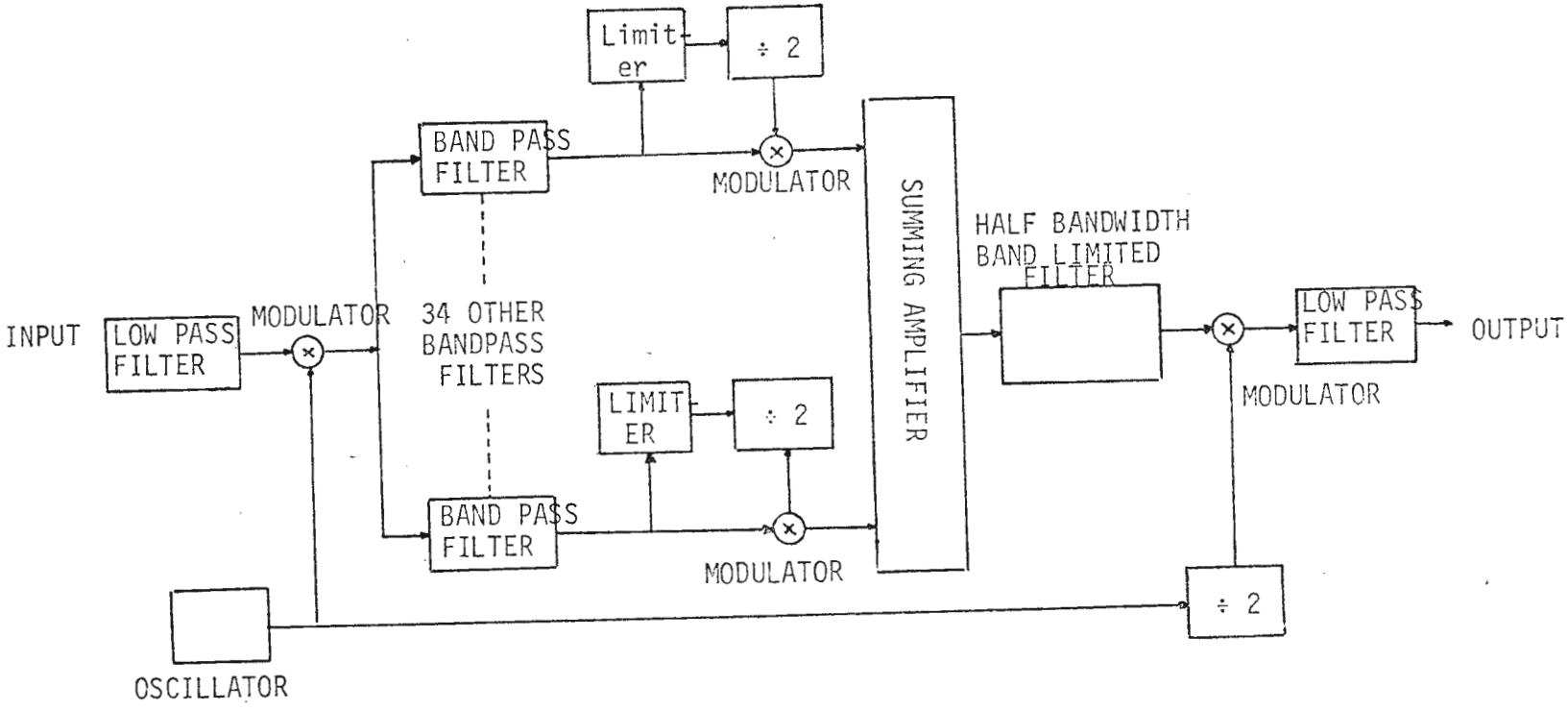


Figure 6. Block Diagram of the Harmonic Compressor.

contains timing logic which prevents simultaneous application of read-in and read-out pulses to the buffer by delaying, when necessary, the read-in pulse. The read-in pulse is generated by the timing logic for each end-of-conversion (EOC) pulse from the analog to digital converter. The read-out pulse is likewise generated by the timing logic for each positive-going transition of the VCO signal. The size of the buffer queue as monitored by sensing the location of a ONE in the forward shift register. The ONE bit is shifted in the forward direction for a read-out pulse and in the reverse direction for a read-in pulse. Since each read-in or read-out pulse is equivalent to a word read into or out of the buffer, the location of the reference bit is an indication of queue size, which then is converted to an analog signal by the digital-to-analog converter. The compensator network is essentially an integrator. It attenuates the high frequency components of the queue signal to reduce the output rate variation but amplifies the low frequency components to prevent buffer overflow or underflow. Hence, the signal applied to the VCO varies slowly and is proportional to the gradual increase or decrease in queue length. Consequently, the data transferred from the buffer will have less TBE than the original samples.

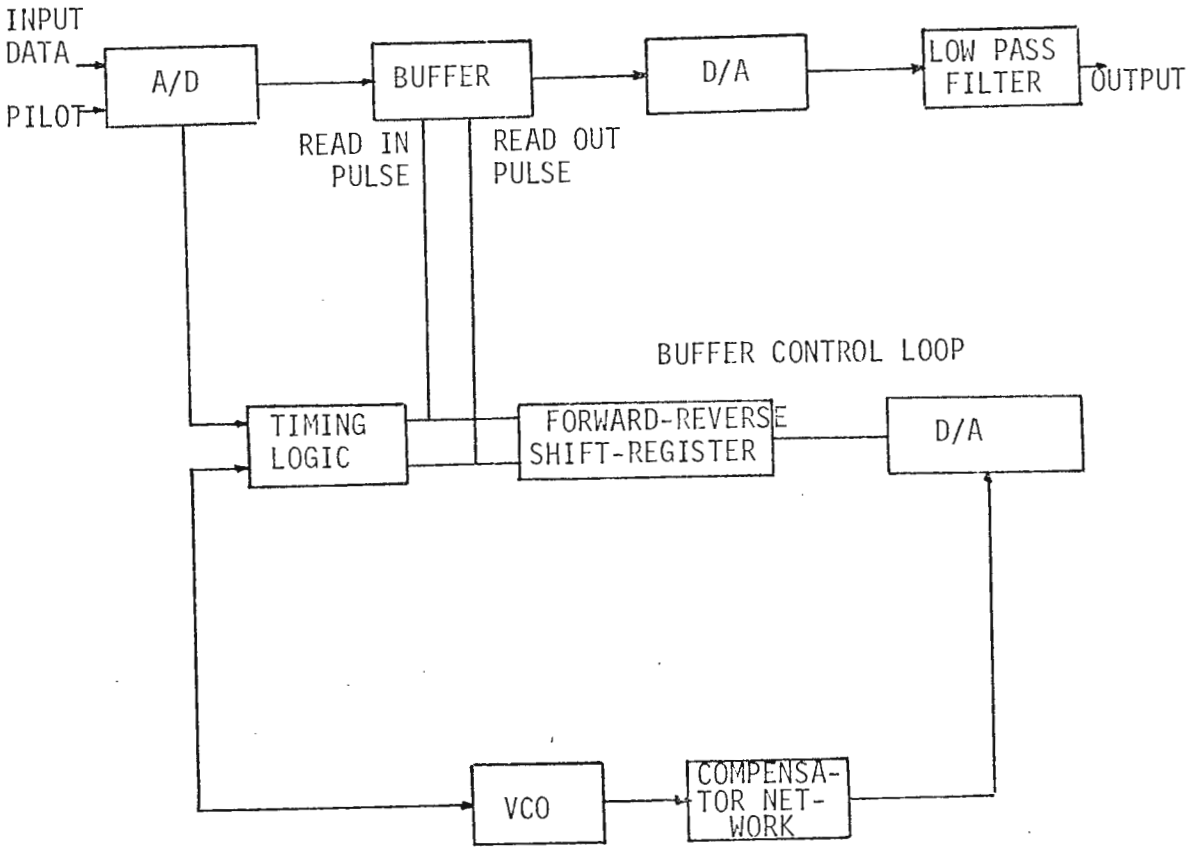


Figure 7. Implementation of Digital TBE Compensator.

II. DESIGN AND MEASUREMENTS OF THE SPEECH EXPANSION/COMPRESSION SYSTEM

A. CIRCUIT DESIGN

The complete block diagram of proposed speech expansion and compression system is illustrated in Fig. 8. The system is designed in three sections. Timing, Driver, and Output.

The timing circuit provides necessary read and store clock pulses for the Bucket Brigades and gate pulses for the multiplexing and demultiplexing circuits.

The driving section includes multiplexing circuits for analog and digital clock signals and the Bucket Brigade's bias circuits.

In the output section there is a demultiplexing circuit which combines the outputs of the two Bucket Brigades.

1. Timing Section Design

Figure 9 illustrates the circuit diagram of the timing section, which provides required clock and gate pulses. In Fig. 9, voltage controlled oscillators are used as frequency sources. Oscillation frequencies of these VCO's are determined by R_1 and R_2.

VCO 1 is used to generate read and store clock pulses. The operation frequency is adjusted as f_c. The output of VCO 1 is applied to the clock input of a JK flip flop whose other inputs are held at the high state. Thus the JK flip flop works as a frequency divider, dividing the output of VCO 1 by two, and $f_c/2$ clock pulses are obtained. When the tape recorder is played back at twice the speed, the compressed signal output of the tape recorder is stored in the Bucket Brigades at clock frequency f_c. The direct output of VCO 1 is used as a store

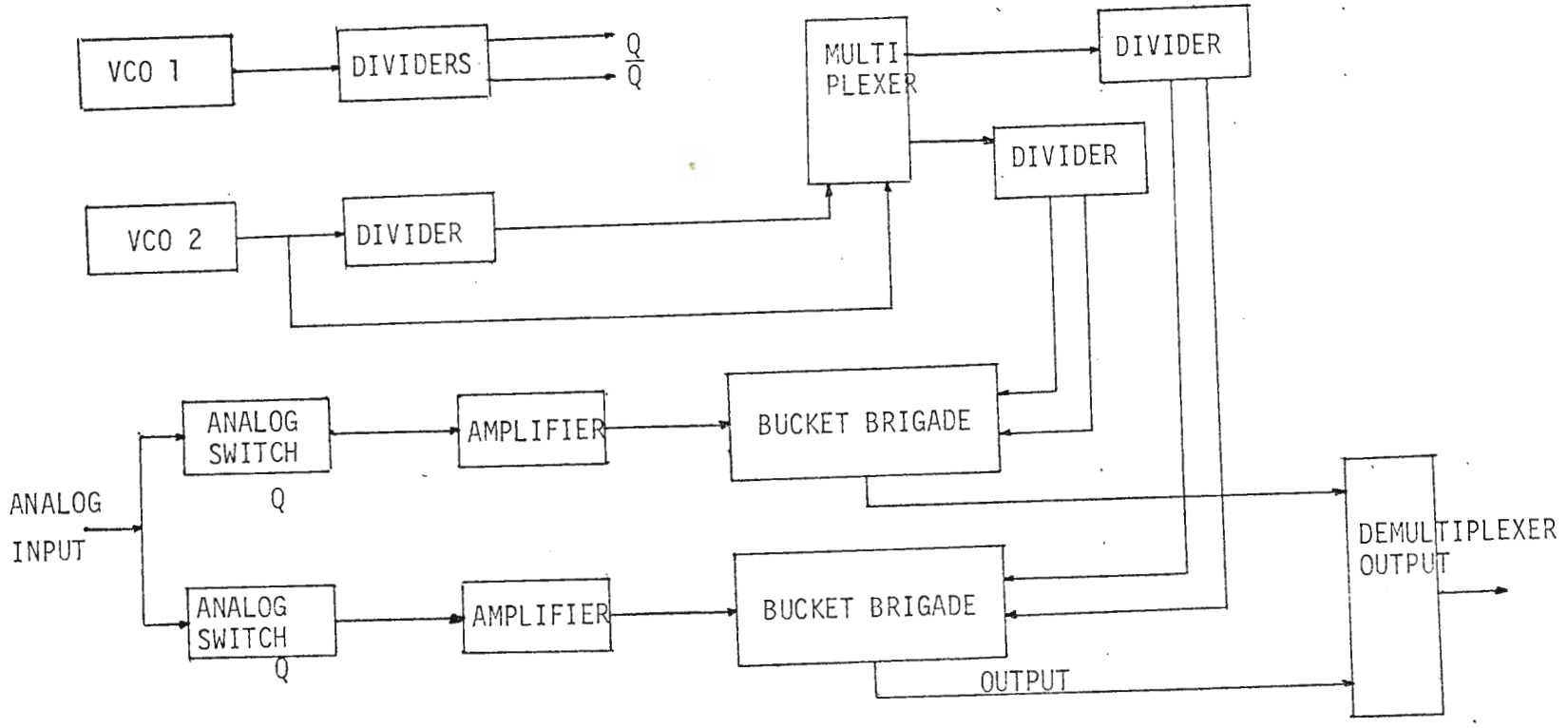


Figure 8. Complete Block Diagram of Speech Expansion and Compression System.

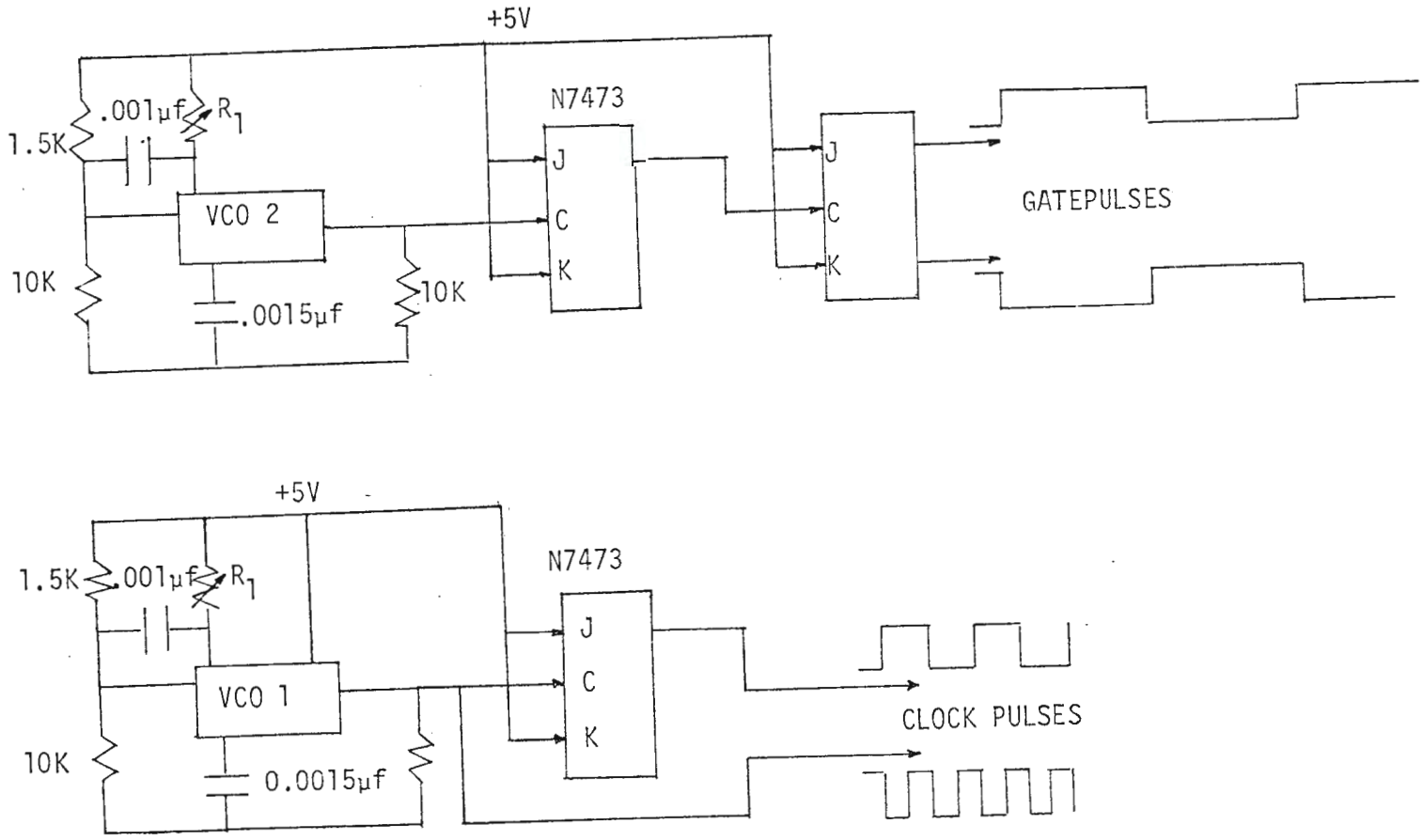


Figure 8. Timing Circuit Diagram.

clock frequency, and the precompressed signal is read out and expanded by the frequency $f_c/2$, which appears at the output of JK flip flop.

When the tape recorder is played back at half speed, the output of the JK is used as the store clock frequency while the output of VCO 1 becomes the read frequency.

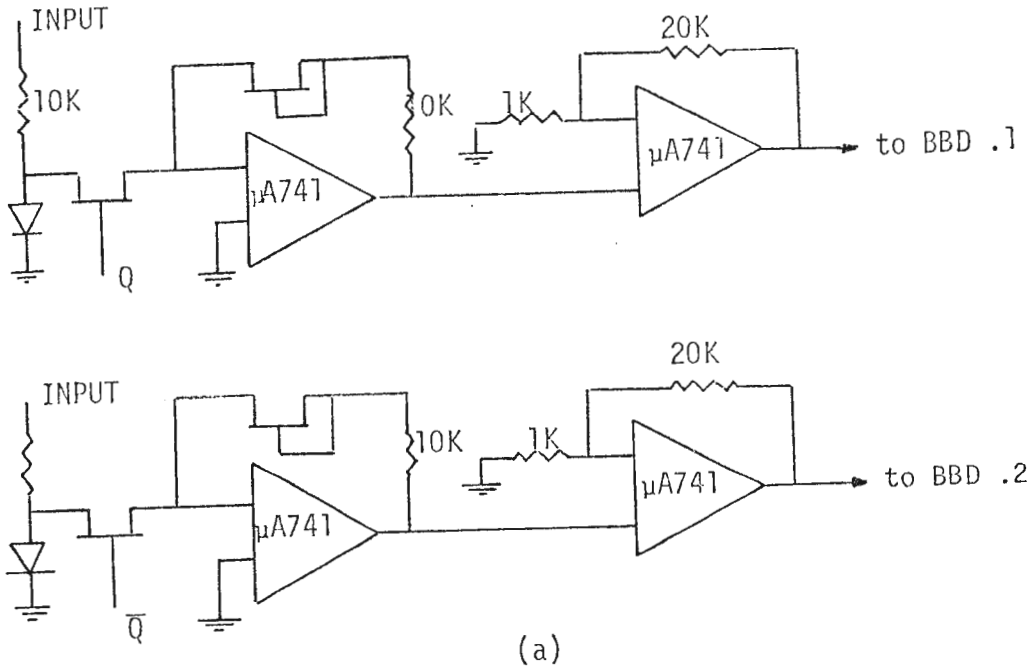
VCO 2 is the source of gate pulses. These pulses are applied to the analog switches and AND gates in the analog and digital signal multiplexing circuits. Duration of the gating pulse must be adjusted to equal the time delay obtained by frequency $f_c/2$. This is defined as $T=32/f_c$ (assuming the Bucket Brigades have 32 bits).

Since the VCO is not stable enough at the gating frequency, the approach used is to operate it at a higher frequency. The output is then divided by 16 using two dual JK flip flops to reduce the frequency to the desired value. The complementary outputs of the last JK are used to gate the analog and digital signals on and off.

2. Driving Section Design

This is the largest and the most important part of the system, including analog and digital multiplexing circuits. Bucket Brigades and associated bias circuits are also included in this section.

In Fig. 10. a, multiplexing circuits for the analog signals are illustrated. Intersil's IH 5010 type analog switches are used, and the output of the tape recorder is applied to the two analog switches simultaneously, but the gate pulses are applied 180 degrees out of phase. Thus, only one of the analog switches (which gets positive gate pulse) passes the input signal. The output of the tape recorder is multiplexed between the two Bucket Brigades in response to timing signals.



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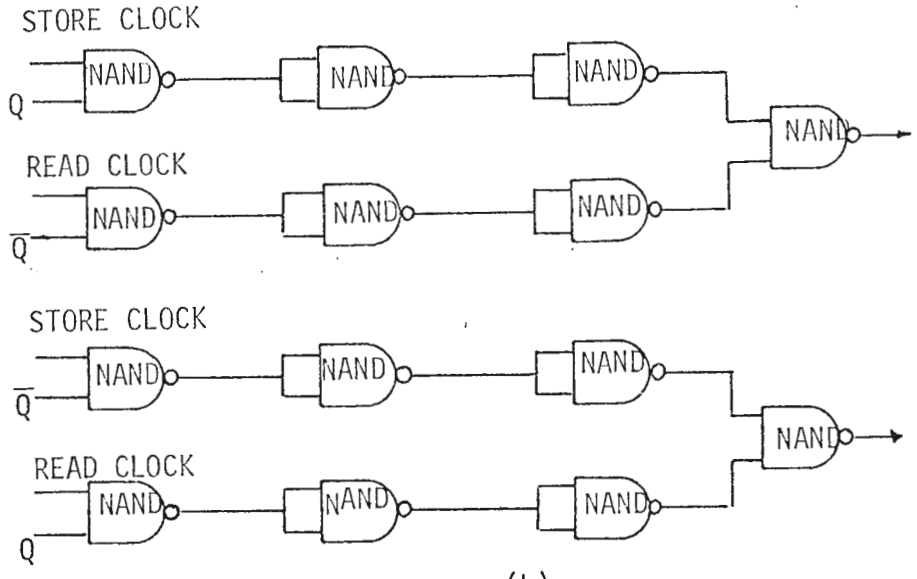

(b)

Figure 10. Multiplexing Circuits for Analog and Dipital Signals.

Fairchild's high performance operational amplifiers (μA 741) function as buffers and amplifiers at the output of the analog switches. Since the input level of the switches is limited to the .7 volts, and this level is not appropriate for the Bucket Brigades, amplification is necessary. At the second operational amplifiers the signal is amplified to ± 2 volts peak.

Multiplexing circuits for read and store clock pulses are illustrated in Fig. 10.b. The circuit functions as follows: When one of the analog switches is gated on, the corresponding Bucket Brigade is switched to the store mode of operation by the store clock pulses. At this moment, the other Bucket Brigade is switched to the read mode of operation, and read clock pulses are applied. Thus, store and read pulses are multiplexed between the Bucket Brigades in response to the gating pulses.

In Fig. 10.b, model 7400 quadruple 2 input positive NAND gates are used as AND and OR gates. The circuit consists of 4 AND and 2 OR gates. Read and store pulses are applied to the Bucket Brigades through these gates. Since the AND gate has an output when both inputs are high, clock pulses can be switched by gate signals. Thus clock and gate pulses are applied to the AND gate simultaneously. When one of the Bucket Brigades is to be switched to the store mode, the corresponding AND gate with store clock pulses is switched by a positive gate pulse. Then the store clock pulses are applied to the Bucket Brigade (which is in the store mode of operation) during the gating period. Conversely, the other Bucket Brigade is in the read mode of operation. The AND gate with read clock pulses has been switched by the same gate pulse. At the end of the gating period, the Bucket Brigades reverse their operation via a new gate pulse.

OR gates are used after the AND gates to prevent loading between them. When one of the AND gates is switched to pass the clock pulses, the output of the other AND gate is always low. This loads the output of the gated (positive) AND gate. OR gates have high outputs when one of the inputs is high and hence the inputs to the Bucket Brigade will be well isolated.

The output of the OR gates are applied to the JK flip flops to obtain the required complementary clock pulses for the Bucket Brigades. The flip flops also work as frequency dividers, a fact which must be considered when determining the operating frequency of VCO 1. The outputs of JK's are positive pulses, but the Bucket Brigades need -10 v. pulses. Therefore, single transistor inverters are used to change the sign and DC level of the clock pulses. In the inverter circuit the transistor is biased at cutoff when there is no input. With the pulse applied to the base, the transistor is driven into the saturation. High speed PNP 2N2905 transistors are used for this purpose. Fig. 11 illustrates the inverters and their associated circuitry.

In Fig. 12 the circuit diagram of the Bucket Brigades are given together with the pin numbers.

Due to the fact that the input signal is sampled and that the samples are measured with respect to ground, the AC input signal needs a DC bias as indicated in Fig. 12. This function is carried out by R_1. The position of R_1 is determined by checking the output signal. When clipping occurs it must be same for the upper and lower sides of the signal. The input AC signal together with the DC bias is connected to pin 6.

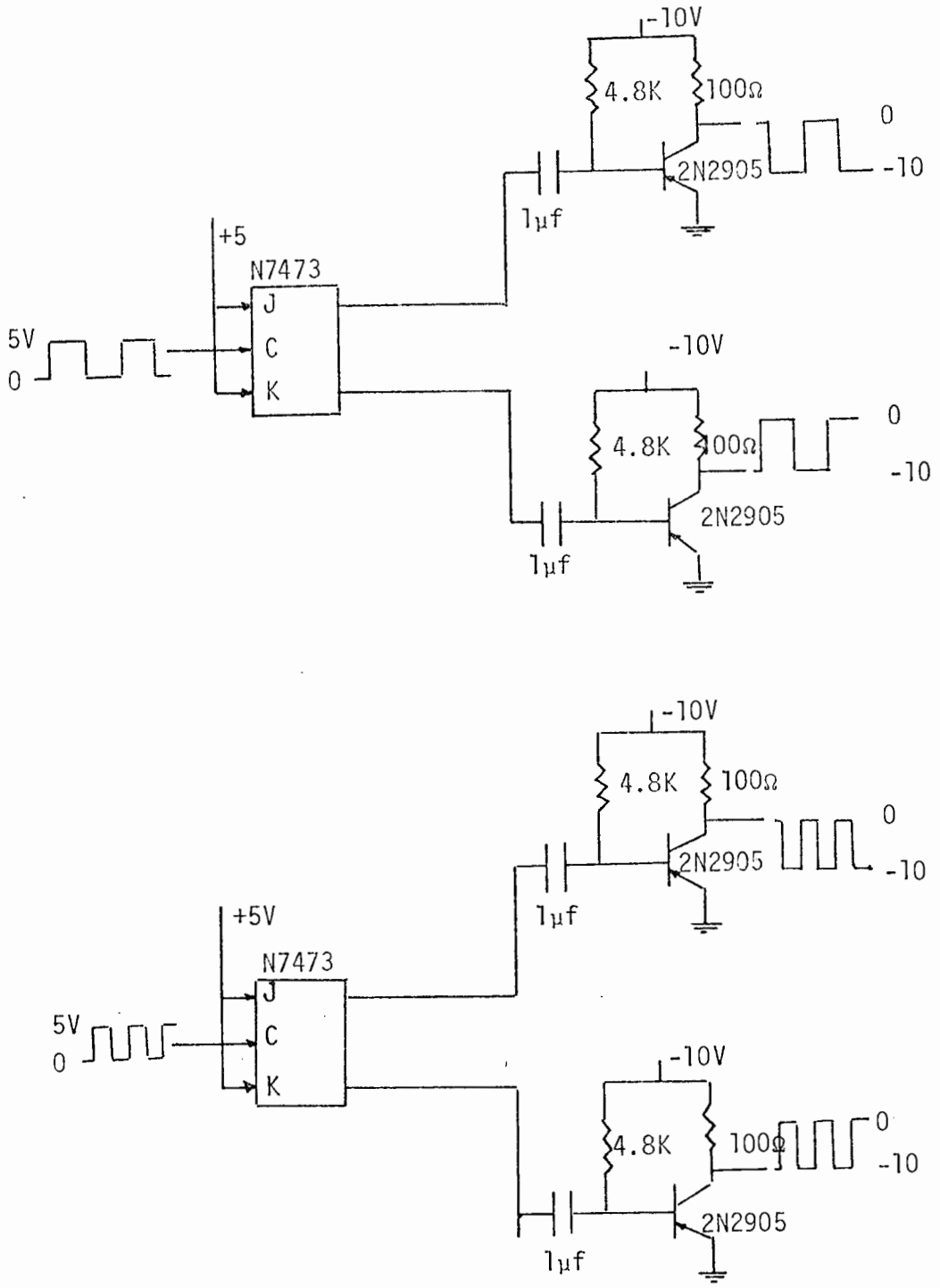

Figure 11. Divider and Inverter Circuits.

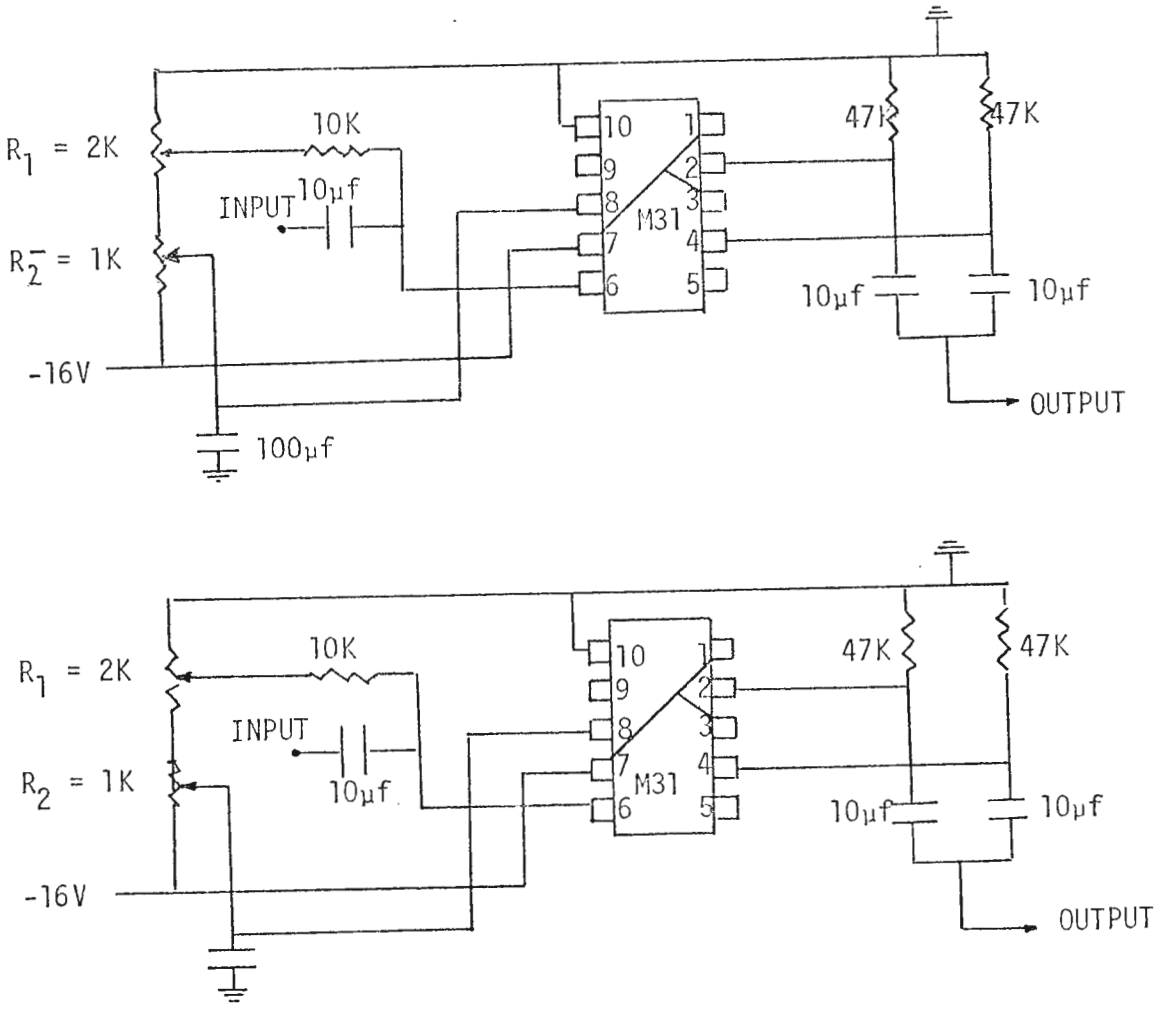

Figure 12. Bucket Brigades Circuit Diagram

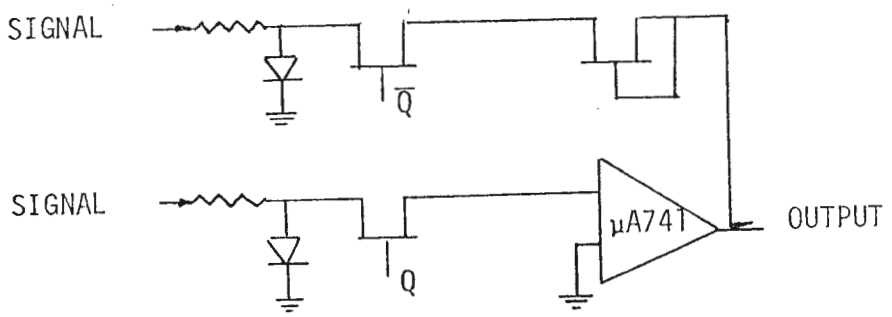

Figure 13. Demultiplexing Circuit Diagram.

Integrated circuit M31 has a tetrode configuration, which means that between two stages an extra MOS transistor is used to avoid interaction. The gates of all of these transistors are connected and bonded on pin 8. Their gates need a DC supply voltage and this is provided through R_2. The value of this voltage is 1 volt less than the clock voltage, and is applied to the connections 5 and 9.

In Fig. 12, pin 1 is connected to the negative supply, pins 2 and 4 are connected to ground through 47 K resistors, and to the output with two capacitors of 10 µf each. The reason that two connections (pins 2 and 4) are used is that the pin 4 acts as a hold circuit for the information on pin 2 during the time the last capacitor is recharged to the reference level. Finally pin 3 and 7 must be connected to the supply voltage.

Internally all odd gates are connected and bonded to pin 9, the even gates being connected to pin 5.

All connections on the input and the output and all interconnections were kept very short to avoid parasitic feedback which could have resulted in ripple on the frequency characteristics. Some troubles may occur when the IC substrate is not well connected to the package. This can be checked for by measuring the resistance between pin 10 and the case. If the resistance is higher than a few ohms, one can solder pin 10 to the package externally.

3. Output Section Design

Figure 13 shows the demultiplexing circuit which combines the outputs of two Bucket Brigades. In this circuit Intersil's IH 5010 analog switch is used. The outputs of the Bucket Brigades are applied to the two channels. The gate pulse which switches the Bucket

Brigades into the read mode of operation also gates the corresponding demultiplexing channel.

B. PRESENTATION OF DATA

The speech expansion and compression system was constructed as described at the preceding section. The system consist of three printed circuit boards with Timing, Driver, and Demultiplexing sections.

After the construction, it was tested for expansion and compression of various forms of analog signals. The results are presented below.

First, the system as used to compress 700 Hz triangular signals. These signals were stored to the Bucket Brigade in sampled form and compressed to 1400 Hz in the read mode of operation of them. Fig. 14 illustrates the input and output wave forms. As was discussed in the proposed approach section, there exists an empty frame due to unequal store and read time.

In Fig. 15, the time compression of the bipolar pulses are shown. 700 Hz bipolar pulses are compressed in time to result in frequency doubling.

In Fig. 14 and 15, to compress the analog signals, the store and read clock frequencies were adjusted as $f_c/2$ and f_c respectively. Since the signals were read out with a faster clock frequency, time compression was obtained.

Figure 16 illustrates expansion of a 700 Hz. sine wave to 350 Hz. Here the output wave form was applied to a low pass filter. Thus, it is not in the sampling form.

To expand an analog signal, it is stored in the Bucket Brigade by clock pulses at f_c, and then read out by the half rate which is $f_c/2$. Due to the low reading rate, signal time expansion was resulted.

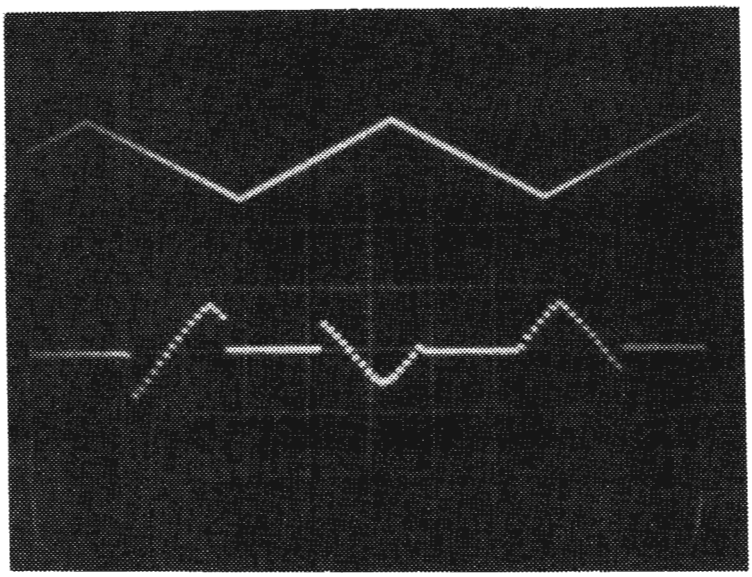

Figure 14. Compression of Triangular Signals.
(Input-upper trace and output-lower trace).

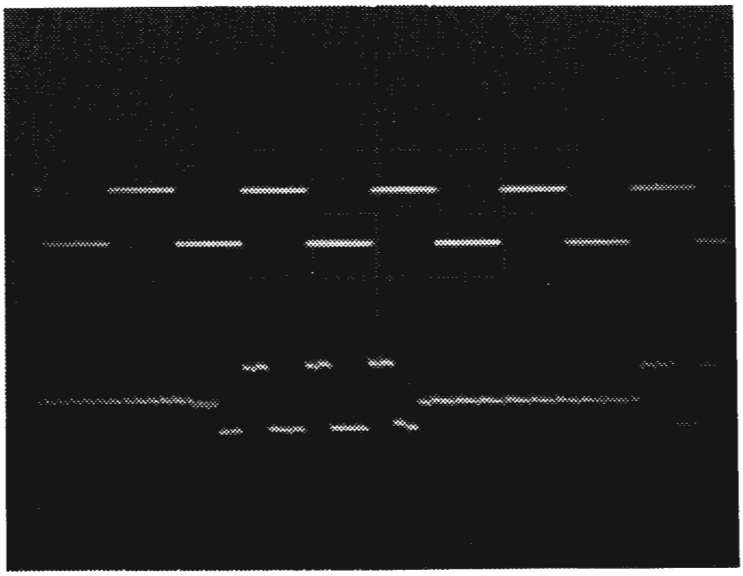

Figure 15. Compression of Bipolar Pulses.
(Input-upper trace and output-lower trace)

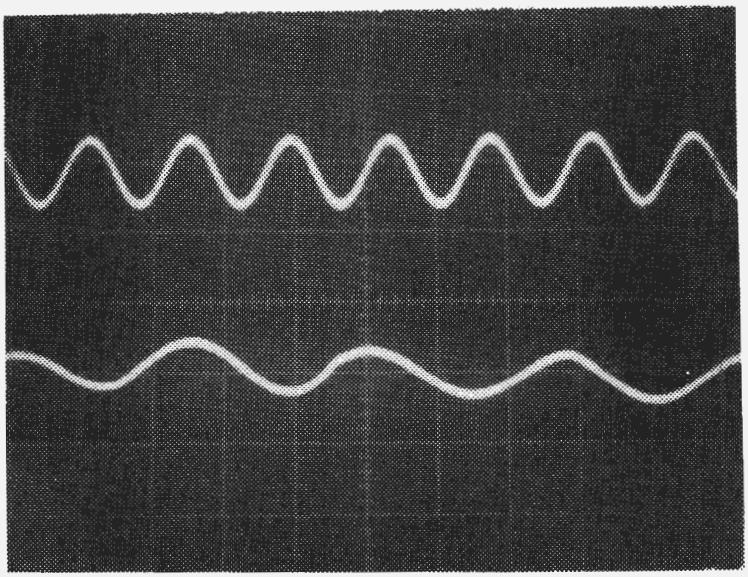

Figure 16. Expansion of Sine Wave.
(Input-upper trace and output-lower trace)

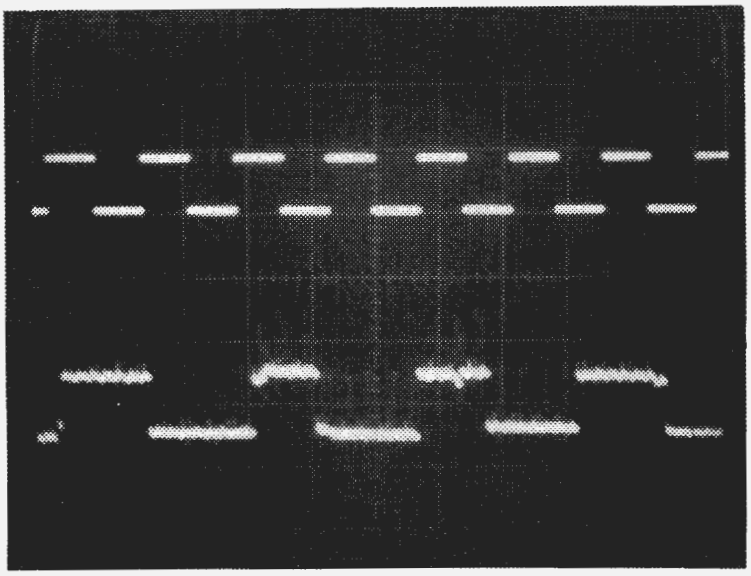

Figure 17. Expansion of Bipolar Pulses.
(Input-upper trace and output-lower trace)

In Figs. 17 and 18, the expansion of the bipolar and triangular pulses are shown respectively.

The performance of speech expansion and compression system was also tested by signals applied from a tone burst generator. A different number of pulses were generated and multiplexed between the two Bucket Brigades, then the stored signal samples were compressed or expanded in the read mode of operation.

In Fig. 19, the expansion of three triangular pulses are illustrated.

Figure 20 shows, the expansion of eight triangular pulses. These pulses are applied to the system, and they are halved to .5 times their original frequency. Since eight pulses are applied during the store time, only four triangular pulses are recovered at the output, with the frequency half of the input.

In Figs. 21 and 22, the compression of sine and triangular wave forms are illustrated. These signals were compressed to two times their original frequency. Again the existance of the empty frames were observed.

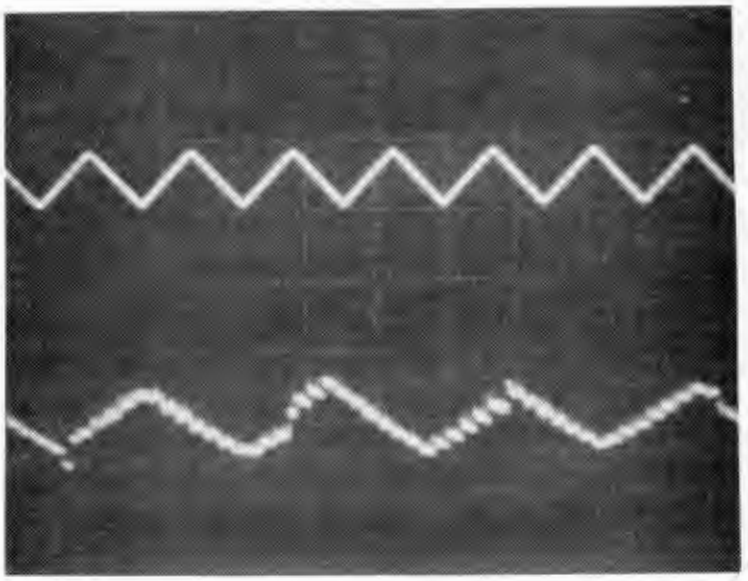

Figure 18. Expansion of Triangular Signals.
(Input-upper trace and output-lower trace)

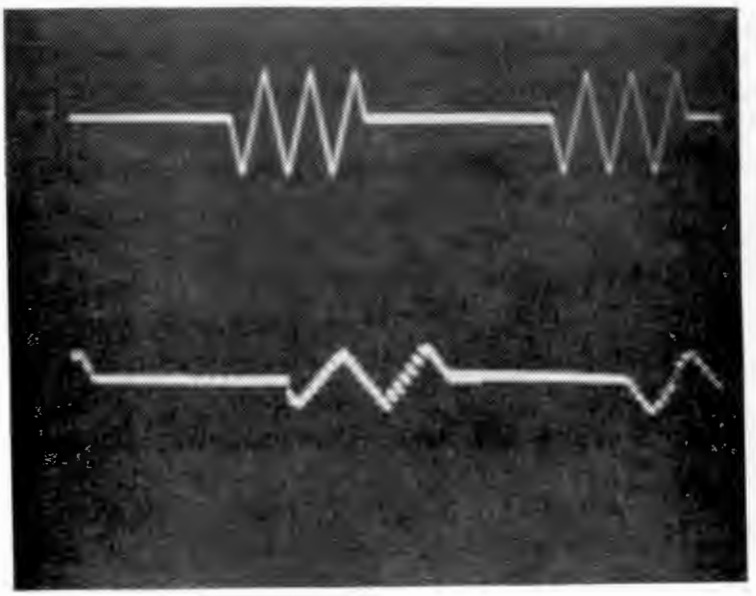

Figure 19. Expansion of Three Triangular Pulses.
(Input-Upper trace and output-lower trace)

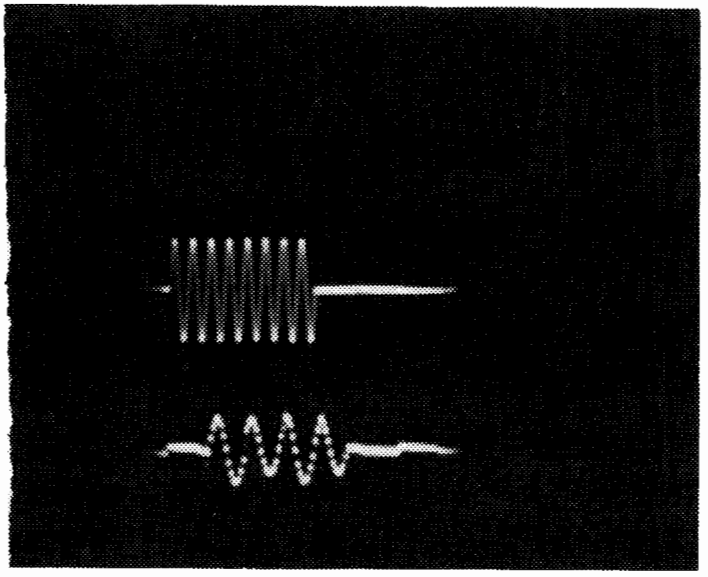

Figure 20. Expansion of Eight Triangular Pulses.
(Input-upper trace and output-lower trace)

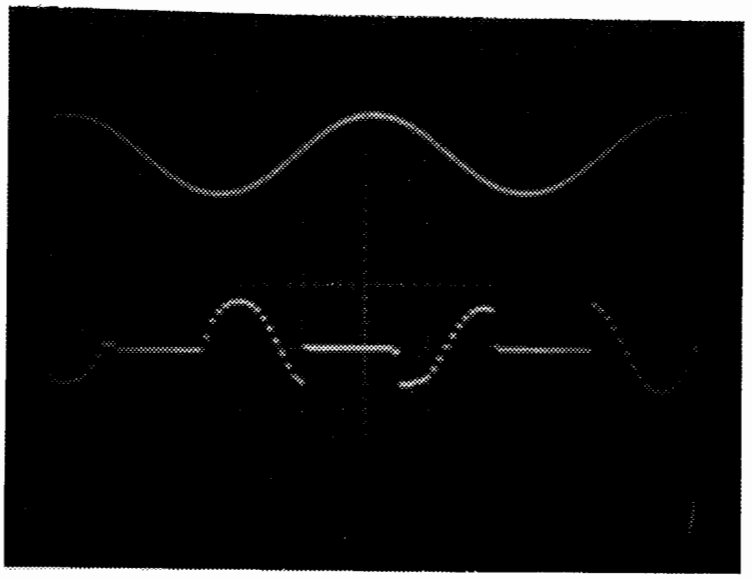

Figure 21. Compression of Sine Wave.
(Input-upper trace and output-lower trace)

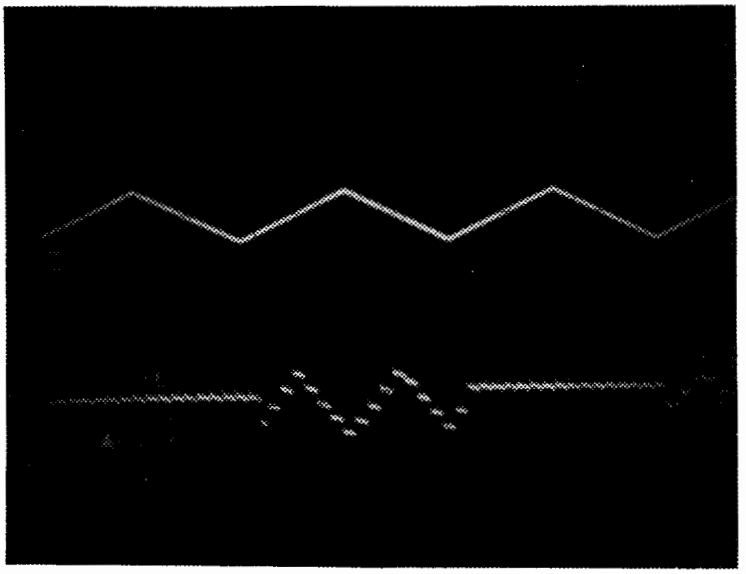

Figure 22. Compression of Triangular Pulses.
(Input-upper trace and output-lower trace)

III. CONCLUSION

The experimental results obtained from the designed speech expansion and compression system demonstrate that the use of a new variable delay principle offers a new inexpensive, simple and important alternative to the existing expensive and complex techniques being used in the field of speech processing.

The performance of the system is consistent with theoretical predictions discussed in the previous sections. It was tested by various forms of analog signals, and they were successively expanded and compressed to their half or two times the original frequency. By the results of tests, it is concluded that in this system, recorded speech which is played back at 1/2 or 1/4 and 2 or 4 times the original rate, can be recovered to its original recording.

IV. RECOMMENDATIONS FOR FURTHER STUDY

The disadvantages of the designed speech expansion and compression system are tabulated, and recommended improvements are discussed below.

First in the system, two voltage controlled oscillators are used as sources of clock frequencies. The oscillation frequencies of these VCO's must be always kept synchronized, but it is too difficult to maintain. If synchronization is lost, the store and read times cannot be adjusted properly. The result is distorted output. Due to improper read and store times, the signal to be expanded cannot be completely read out by the read clock pulses, thus, at the output, some portions of signal appear without expansion. Conversely, in compression, due to the same problem, some portions of the output appear without being compressed.

To overcome this disadvantage, one should use only one voltage controlled oscillator as sources of clock and gate frequencies. The operation frequency of the VCO can be divided by several JK flip flops to obtain required gate pulses. Since JK flip flops have fan-out limits of about ten, this will not introduce any problem.

The size of the system can be reduced if multiplexing (for the analog and digital signals) and demultiplexing circuits are omitted. This is possible by proper connection of the two Bucket Brigades. Figure 23 illustrates the block diagram of the proposed connection. In this figure, the output of the tape-recorder is stored in the first Bucket Brigade at the store clock frequency. The signal is stored in the device in the form of samples. These samples are then transferred to the other Bucket Brigade by the same clock pulses. But the samples arriving at the second device are then clocked and proceed to the output

by the read clock pulses. That is each sample is transferred in the second Bucket Brigade with a rate lower or higher than its sampling rate. Obviously, the read pulses can be adjusted to compress or to expand the signal coming from the first Bucket Brigade. If the read pulses are adjusted to half of the store clock frequency, the signal samples are then transferred in the second device with a smaller rate. This results signal time expansion.

Since in this system, the signal is always stored in the first Bucket Brigade, there is no need to multiplex.

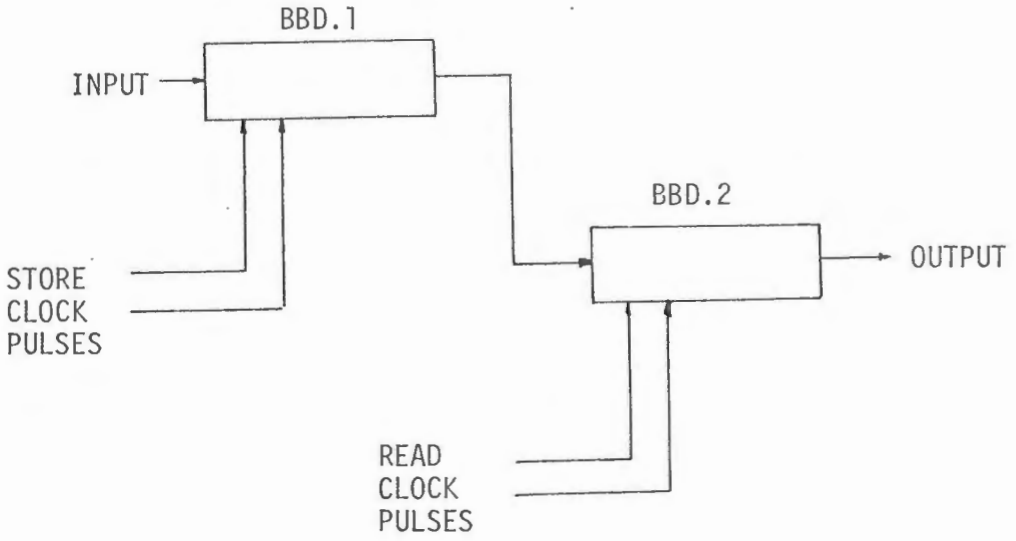

Figure 23. Block Diagram of the Proposed Connection of the Bucket Brigades.

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13. ABSTRACT

A new variable analog delay principle is used during playback, of pre-recorded speech, to maintain the original pitch when it is played back at half and at twice original recording speed. Original pitch is maintained in speeded up or slowed down speech by expanding or compressing in time, respectively.

A proposed system is described and typical experimental results are provided to illustrate the system performance.

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